2

Features

512Kx8 bit CMOS Static
Random Access Memory

- Access Times: 55, 70, 85 and 100ns
- Data Retention Function (LP version)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

32 lead, JEDEC Approved Pinout

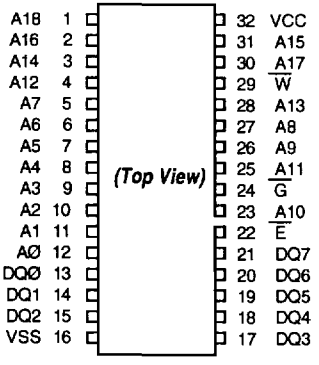
- Ceramic Sidebrazed DIP, No. 9
- Ceramic SOJ, No. 140

Single +5V (±10%) Supply Operation

512Kx8 Static RAM
CMOS, Monolithic

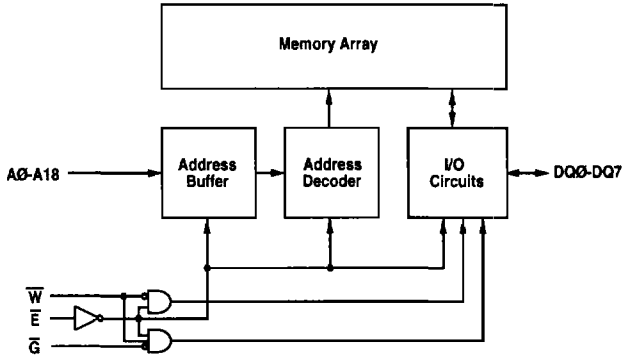
The EDI88512C is a 4 megabit Monolithic CMOS Static RAM. The 32 pin DIP pinout adheres to the JEDEC standard for the four megabit device and is a pin for pin replacement for the 512Kx8 module, EDI8M8512C. Both the DIP and CSOJ packages are pin for pin upgrades for the single chip enable 128K x 8, the EDI88128C. Pins 1 and 30 become the higher order addresses. A Low Power version with Data Retention (EDI88512LP) is also available for battery backed applications.
Military product is available compliant to Appendix A of MIL-PRF-38535.

Pin Configurations and Block Diagram



Pin Names

AØ-A18	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Storage Temperature, Ceramic	-65°C to +150°C
Power Dissipation	1 Watt
Output Current.	20 mA
Junction Temperature, TJ	175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.5	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	See Figure 1

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

Figure 1

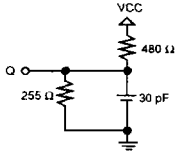
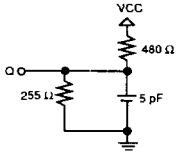


Figure 2



DC Electrical Characteristics

Parameter	Sym	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	W, E = VIL, I/O = 0mA, Min Cycle	70-100ns	--	45	75	mA
			55ns			100	mA
Standby (TTL) Power Supply Current	ICC2	E ≥ VIH, VIN ≤ VIL, VIN ≥ VIH		--	3	10	mA
Full Standby Power Supply Current	ICC3	E ≥ VCC-0.2V	C	--	--	5	mA
		VIN ≥ VCC-0.2V or VIN ≤ 0.2V	LP	--	--	2	mA
Input Leakage Current	ILI	VIN = 0V to VCC		--	--	±10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		--	--	±10	µA
Output High Voltage	VOH	IOH = -1.0mA		2.4	--	--	V
Output Low Voltage	VOL	IOL = 2.1mA		--	--	0.4	V

*Typical: TA=25°C, VCC=5.0V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	12	pF
Data Lines	CD/Q	14	pF

These parameters are sampled, not 100% tested.

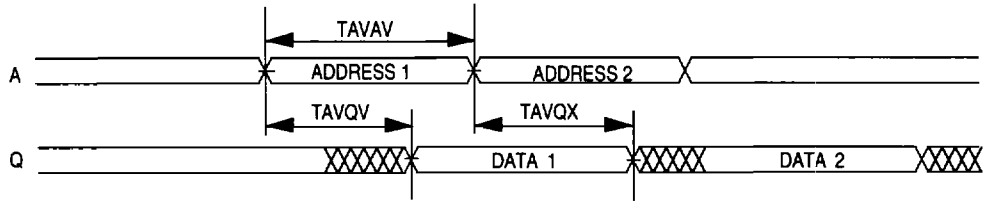
AC Characteristics Read Cycle

	Symbol		55ns		70ns		85ns		100ns		
Parameter	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Units
Read Cycle Time	TAVAV	TRC	55		70		85		100		ns
Address Access Time	TAVQV	TAA		55		70		85		100	ns
Chip Enable Access Time	TELQV	TACS		55		70		85		100	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	10		10		10		10		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		20		25		30		30	ns
Output Hold from Address Change	TAVQX	TOH	10		10		10		10		ns
Output Enable to Output Valid	TGLQV	TOE		30		35		45		50	ns
Output Enable to Output in Low Z (1)	TGLQX	TLOZ	5		5		5		5		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ	0	20	0	25	0	30	0	30	ns

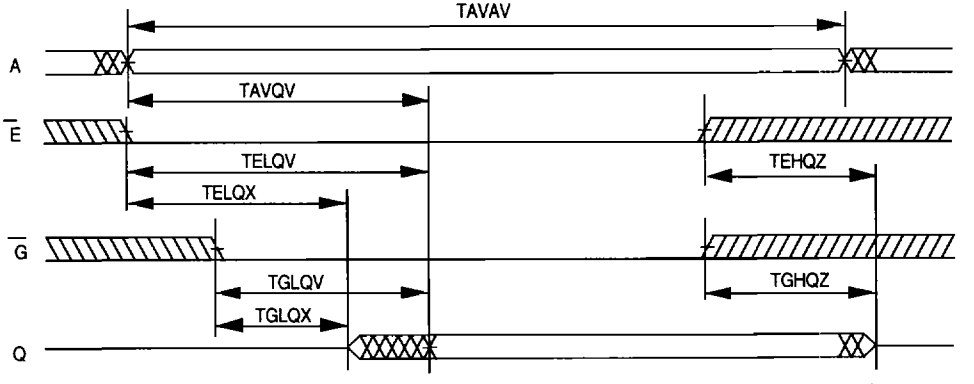
Note 1: Parameter guaranteed, but not tested.

2

Read Cycle 1 - W High, G, E Low



Read Cycle 2 - W High

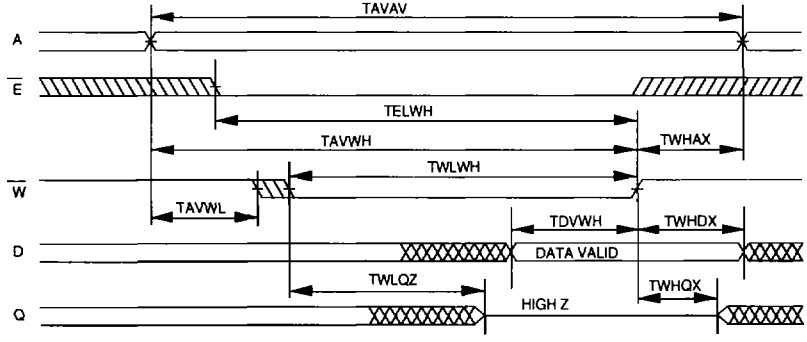


AC Characteristics Write Cycle

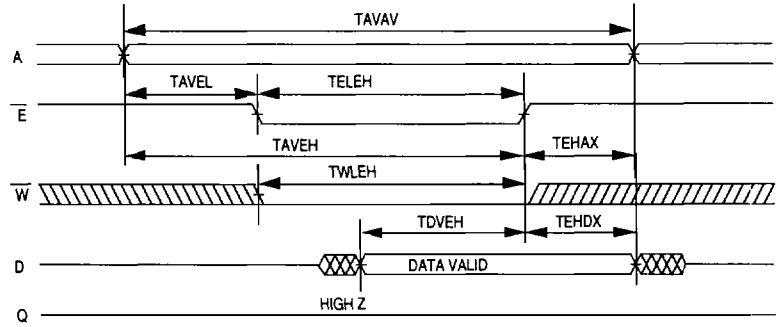
	Symbol		55ns		70ns		85ns		100ns		
Parameter	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Units
Write Cycle Time	TAVAV	TWC	55		70		85		100		ns
Chip Enable to End of Write	TELWH	TCW	50		60		70		80		ns
	TELEH	TCW	50		60		70		80		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	50		65		70		80		ns
	TAVEH	TAW	50		65		70		80		ns
Write Pulse Width	TWLWH	TWP	45		50		55		60		ns
	TWLEH	TWP	45		50		55		60		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		ns
Data Hold Time in High Z (1)	TWHDX	TDH	0		0		0		0		ns
	TEHDX	TDH	0		0		0		0		ns
Write to Output in High Z	TWLQZ	TWHZ	0	25	0	25	0	30	0	30	ns
Data to Write Time	TDVWH	TDW	40		40		40		40		ns
	TDVEH	TDW	30		30		35		40		ns
Output Active from End of Write (1)	TWHQX	TWLZ	5		5		5		5		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - W Controlled



Write Cycle 2 - E Controlled



Data Retention Characteristics

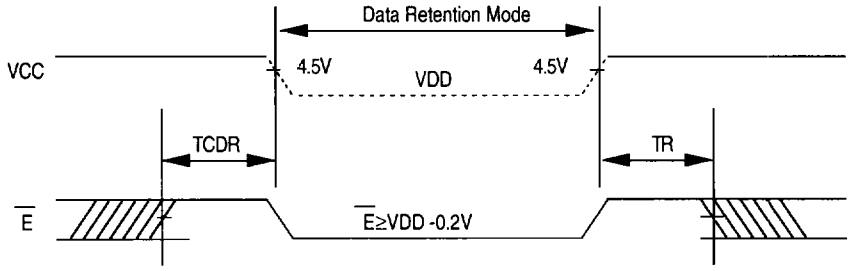
EDI88512LP Only

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max	Unit
Data Retention Voltage	VDD			2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E} \geq$ VDD -0.2V	2V	--	--	185	µA
Chip Disable to Data Retention Time	TCDR	VIN ≥VDD -0.2V		0	--	--	ns
Operation Recovery Time	TR	or VIN ≤0.2V		TAVAV	--	--	ms

*Read Cycle Time

2

Data Retention E Controlled



Ordering Information

Part No. Standard Power	Speed (ns)	Package No.
EDI88512C55CB	55	9
EDI88512C70CB	70	9
EDI88512C85CB	85	9
EDI88512C100CB	100	9
EDI88512C55NB	55	140
EDI88512C70NB	70	140
EDI88512C85NB	85	140
EDI88512C100NB	100	140

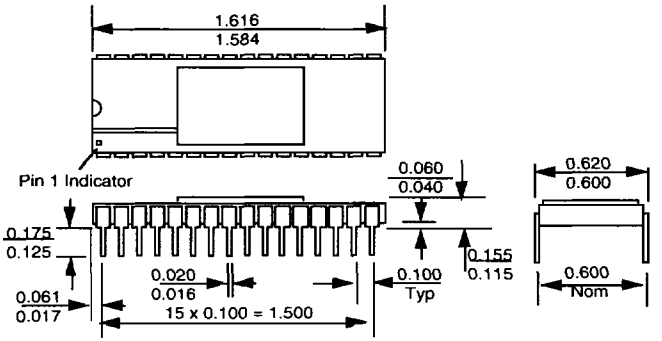
Low Power with Data Retention	Speed (ns)	Package No.
EDI88512LP55CB	55	9
EDI88512LP70CB	70	9
EDI88512LP85CB	85	9
EDI88512LP100CB	100	9
EDI88512LP55NB	55	140
EDI88512LP70NB	70	140
EDI88512LP85NB	85	140
EDI88512LP100NB	100	140

For Commercial, Industrial and Militarygrade product use C, I or M respectively to replace B in the suffix of the part number, eg EDI88512C100CB becomes EDI88512C100CM (Military Temp range).

Package Description

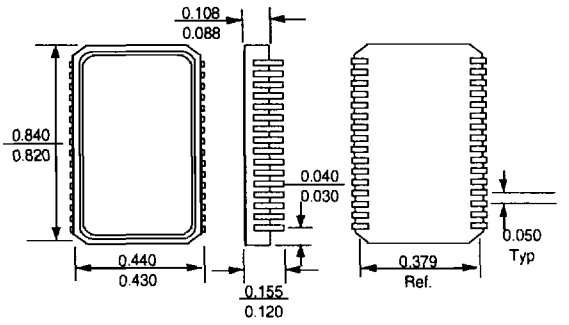
Package No. 9
32 Pin Sidebrazed Ceramic Dual-in-line Package

Weight = 5.80g
Theta J_A = 20°C/W
Theta Jc = 6.5° C/W



Package No. 140
32 Lead Ceramic SOJ Package

Weight = 1.90g
Theta J_A = 40°C/W
Theta Jc = 8° C/W



Electronic Designs Incorporated
• One Research Drive • Westborough, MA 01581USA • 508-366-5151 • FAX 508-836-4850 •
Electronic Designs Europe Ltd. • Shelley House, The Avenue • Lightwater, Surrey GU18 5RF
United Kingdom • 01276 472637 • FAX: 01276 473748